Prof. Samary Baranov

Bar Ilan University/School of Engineering, Ramat Gan, Israel

samary@bell.net baranos@eng.biu.ac.il

High Level Synthesis of Digital Systems

(New design methodology and tool)

The tremendous achievements in the integral technology allow to produce chips with several millions elements. At the same time, the design technology of such circuits didn't change practically during last ten years. The traditional design flow for digital system design contains the hand creation of Verilog or VHDL code. As a result, the time-to-market for systems on such chips is increased by factor two-three. The only possibility to reduce a gap between designer's productivity and future technological capability is to raise the design from the current register transfer level to the algorithmic or behavior level.

The main goal of this technical seminar is to present a new methodology for high level and logic design of very complicated digital systems. This methodology, implemented in EDA (Electronic Design Automation) tool Abelite, is based on Algorithmic State machine (ASM) transformations (composition, minimization, extraction, etc.), special algorithms for Data Path, Control Unit and Top design and a very fast optimizing synthesis of FSM and combinational circuits with hardly any constraints on their size, that is, the number of inputs, outputs and states. Design tool Abelite supporting this methodology allows very fast to implement, check and estimate many possible design versions, to find an optimized decision of the design problems and to simplify the verification problems for digital systems.

The content of this lecture:

1. Demonstration of EDA tool Abelite supporting a new design methodology and implementing *fully automatic* high level synthesis of digital systems;
2. Presentation of the logic synthesis in Abelite. We will show that Abelite reduces the circuit area of very complicated Finite state machines and combinational circuits by as much as 50%, compared with results of the best USA industrial tools from Synopsys, Xilinx, Altera and Mentor Graphics and yet the run times of these other tools exceed that of Abelite by more than a factor of 10.